

A CMOS Variable Width Short-Pulse Generator Circuit for UWB RADAR Applications

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Abstract—This paper describes a variable width short pulse generator circuit for UWB radar applications, designed in a 0.18 μm CMOS technology. This circuit is capable of generating pulses with a duration from 0.7 ns to 3.5 ns and an amplitude of 0.7 V with a 50 Ω load. The power supply voltage can be as low as 1.5 V and uses only 2.3 mA of power supply current.

I. INTRODUCTION

The use of UWB radar systems for imaging applications is regulated by the FCC. These regulations specify the frequency bands and power levels allowed for radar systems [1]. In particular, they allow to use UWB signals in the frequency band between 0 Hz and 960 MHz. The possible applications of these UWB radar systems include ground penetrating RADARs (GPRs), and through-wall imaging systems.

An UWB radar system [2], [3] works by transmitting an electromagnetic pulse with a short width (equal to T_p) and detecting the reflections (echoes) created by this pulse on the targets. The radiated pulse travels at the speed of light and when it encounters a dielectric transition (target) an echo signal is created. The distance (or range) to the target, is directly related to the travel time (T) of the signal, from the transmitter to the target and back to the receiver. The target range is calculated multiplying $T/2$ by the speed of light. The transmitted pulse is periodically transmitted with a given pulse repetition frequency (PRF). The spectrum of the pulse signal applied to the antenna consists of narrow spectral lines, located at multiples of the PFR. The amplitude of these spectral lines is determined by a *sinc* function with the first zero at approximately $1/(T_p)$. This spectrum is filtered by the antenna transfer function, which acts as a band-pass filter, essentially determining the radiated pulse shape. Therefore, the spectrum of the radiated signal is determined by the type of antenna and by the width of the UWB pulse. Since, it is very difficult to change the characteristics of the antenna, the only available option to change the spectrum content of the radiated signal is to adjust the value of the pulse duration (T_p).

In this paper a CMOS circuit capable of generating short pulses with variable pulse duration is presented. The circuit is capable of generating short pulses with a width between 0.7 ns and 3.5 ns with 0.7 V of peak amplitude on a 50 Ω load.

II. PRINCIPLE OF OPERATION

The objective of the circuit is to create a short pulse with a variable width. A simple circuit capable of generating short pulses is constituted by an AND gate where one input is connected to a clock signal and the other input is connected to a delayed version of the clock signal. The shape of the pulse is determined by the rise and fall times of the AND gate together with the load of the circuit (the antenna). However, this simple circuit has a problem: it creates pulses both on the rising and falling edges of the clock signal. In order to eliminate this problem, it is necessary to use an edge triggered flip-flop. When the rising edge of the clock appears the flip-flop changes its output signal from “0” to “1”. This output is connected to the asynchronous reset of the flip-flop through a variable delay element, causing the output signal to change from “1” to “0” after the delay time. The end result is an approximately rectangular short pulse, produced only in the rising edge of the clock signal. This circuit is shown next in Fig. 1.

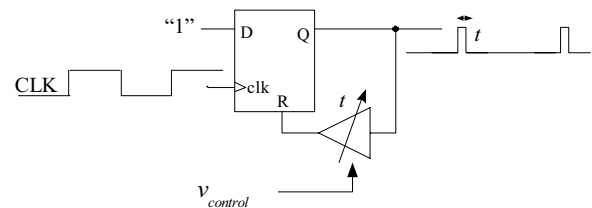


Figure 1. Simplified block diagram of the short pulse generator circuit.

The width of the pulse is controlled by the amount of delay created by the variable delay buffer. This delay is determined by a control voltage. If this circuit is to be integrated together with an UWB receiver channel, it is necessary that the switching noise produced by this circuit be as low as possible, in order to improve the sensitivity of the receiver. Therefore, the circuit is implemented using circuits based on differential logic, this type of circuits operate in class A and therefore create a minimum amount of current peaks in the power supply lines (the bias current is constant). However, if these type of circuits were to drive directly a small impedance (such as the antenna) it would be necessary to use a differential buffer with large bias current value in order to obtain small

rise and fall times and a large signal amplitude. Since the clock frequency (PRF) is low (typically below 5 MHz), it is more efficient to use a CMOS output buffer, because CMOS circuits only draw current during the voltage transitions of the signal. A CMOS buffer uses, on average, much less current than a differential buffer with the same rise and fall times on the same load. In order to use a CMOS buffer it is necessary to convert the output differential signal of the flip-flop into a CMOS signal, using a differential to CMOS level conversion circuit. The output of this circuit is then connected to two CMOS inverters (with an increasing driving capability) before driving the antenna. The input clock signal must also be converted from a CMOS digital signal into a differential digital signal using a CMOS to differential level conversion circuit.

III. DIFFERENTIAL LOGIC CIRCUITS

The basic building block of the differential logic is the buffer (or inverter circuit) composed by a differential pair and a resistive load, depicted next in Fig. 2.

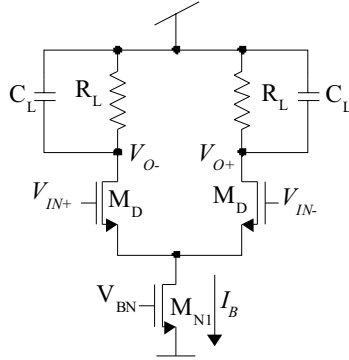


Figure 2. Figure 1. Differential buffer schematic.

This buffer operates with differential digital signals, whose voltage levels correspond to the buffer's two differential output voltage levels when the differential pair is saturated (one of the transistors M_D is ON and the other is OFF). The value of the buffer differential output voltage swing (V_{swing}) is determined by the buffer bias current (I_B) and by the load resistance value (R_L). The amplitude of the output voltage swing (V_{swing}) of the differential buffer depends on the values of the output resistance and bias current. The output resistance can vary with process and temperature up to 30% of its nominal value. This variation can be compensated using a negative feedback loop to adjust I_B in order to maintain a constant output voltage swing. It would be difficult and inefficient to realize this adjustment inside every differential buffer of the circuit. The feedback circuit would add power dissipation to each buffer and it would be necessary to eliminate the differential signal from its feedback path. It is more efficient to have a replica of the buffer circuit (actually only half of the buffer circuit is needed since one of the outputs is V_{DD}) and adjust the output amplitude of this circuit to be equal to the desired value of the voltage swing. The bias current of this half-buffer can then be mirrored to all the buffer circuits [4]. This principle is shown next in Fig. 3.

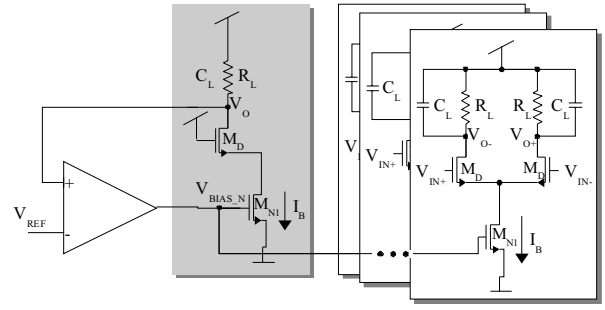


Figure 3. Replica bias principle.

The replica bias circuit works by comparing the reference voltage (V_{REF}) with the half-buffer output voltage (V_O) using an amplifier. The amplifier output voltage (V_{BIAS_N}) determines the value of I_B . The amplifier adjusts the value of this current until the output voltage is almost equal to the reference voltage, therefore $V_{REF} = V_{swing}$. The relative error between V_{REF} and the V_O depends on the feedback loop gain of the replica bias circuit and is not critical, since V_{swing} is chosen to have a safety margin of at least 10% over the saturation voltage of the differential pair in the buffer circuit. A loop gain larger than 32 dB is enough to have an error smaller than 2.5%. The V_{BIAS_N} voltage of the replica bias circuit is applied to the M_{N1} transistors of the differential buffers, generating a bias current inside these buffers equal to the bias current of the half-buffer replica circuit. Thus, the buffers have an output voltage swing with the same value as the V_O voltage of the half-buffer in the replica bias circuit. If the transistors of the differential buffer are scaled to have a larger multiplicity (M) than the transistors of the half-buffer, the bias current of the differential buffer will be M times higher than the bias current of the half-buffer. In this case the load resistance value of the buffer is scaled to R_L/M in order to maintain the buffer output voltage swing equal to V_{swing} .

The variable delay circuit in reset path, is a differential buffer where the load resistances are replaced by PMOS transistors in the linear region. The control voltage V_{BIAS_P} is applied to the gates of these transistors, controlling the value of the load resistance of the buffer (the drain resistance of the PMOS transistors). This allows changing the buffer time constant and therefore the input-output delay of the circuit. In order to maintain the same voltage swing independently of the value of V_{BIAS_P} , it is necessary to use a separate replica bias circuit to adjust the bias current of the variable delay buffer; this is shown next in Fig. 4.

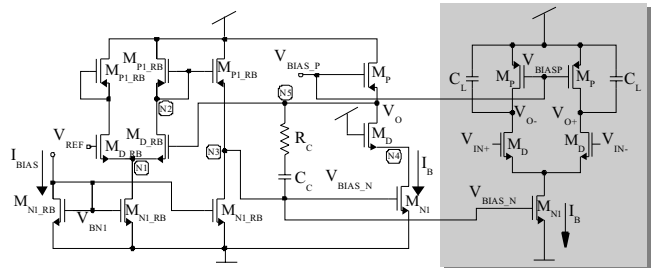


Figure 4. Replica bias circuit with a variable delay buffer schematic.

This replica bias circuit controls only the variable delay buffer, while the first replica bias circuit controls all the differential logic circuits. It should be noted that it is necessary to carefully compensate this feedback loop because the drain resistance of the PMOS transistor can be very high (in the case of a large delay) and therefore the loop gain also become large.

It is possible to obtain differential logic gate, modifying the differential buffer circuit of Fig. 2, by adding a second differential pair. This circuit can realise the four basic logic operations AND, NAND, OR and NOR, depending on how the input and output signals are connected, because realizing a NOT function using differential signals consists simply in reversing the polarity of the signal. As an example, the circuit shown in Fig. 5 is connected as a AND gate; reversing the polarity of the output nodes, would change the circuit into a NAND gate; reversing the polarity of both input signals, would change the circuit into an OR gate (from the Morgan law) and finally reversing the polarity of the output and input signals, would change the circuit into a NOR gate. The flip flop circuit is built using 4 differential NOR gates [5] as shown in Fig. 5.

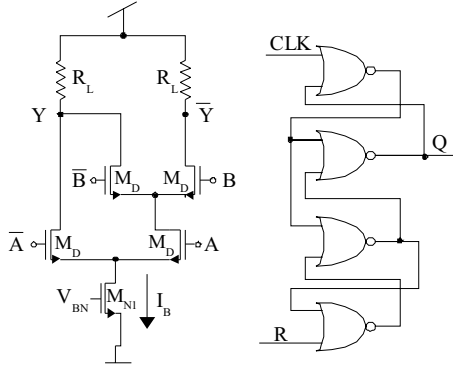


Figure 5. Differential AND gate circuit (on the left side) and flip flop circuit (on the right side).

The differential to CMOS level converter circuit is depicted below in Fig. 6. This circuit is constituted by a two stage amplifier followed by a two CMOS inverters. The amplifier is designed to have a large gain-bandwidth product. The first stage is designed to have a large gain to reduce the systematic offset due to the second stage and the CMOS inverters. Since this amplifier works in open-loop there are no stability problems associated to the design.

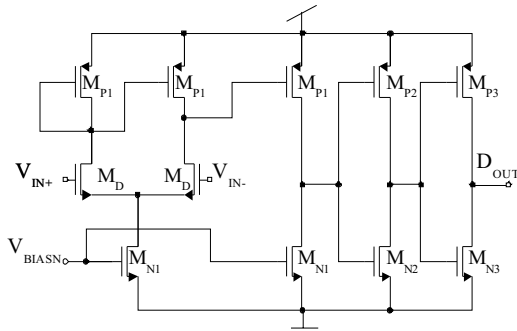


Figure 6. Schematic of the differential to CMOS level conversion circuit.

The complete short pulse generator schematic is depicted next in Fig. 7.

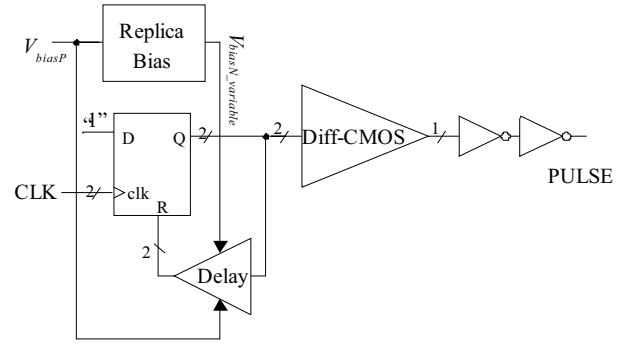


Figure 7. Schematic of the short pulse generator circuit.

The expected supply current of each sub-circuit is shown next in Table 1. These values do not change significantly with the PRF value because most of the circuits operate in class A.

TABLE I. EXPECTED SUPPLY CURRENT OF THE SHORT PULSE GENERATOR SUB-CIRCUITS.

Flip-flop	Replica bias	delay	buffer	buffer	Diff-CMOS	Total
400 μ A	400 μ A	100 μ A	400 μ A	800 μ A	200 μ A	2300 μ A

IV. EXPERIMENTAL RESULTS

In order to measure the output voltage of the short-pulse generator circuit, a 2.5MHz CMOS clock signal with 50% duty cycle is applied to the input clock of the circuit. The output voltage of the circuit is measured using the digital oscilloscope (TDS 3052). This oscilloscope is also used to measure the pulse width and amplitude. The input impedance of the oscilloscope is composed by a 13 pF capacitor in parallel with a load resistance of 50 Ω or 1M Ω , the output signal of the short pulse generator was measured for different values of the bias voltage (V_{BIAS_P}) and for the two load resistance values. As an example, the output voltage waveform of the short pulse generator for a bias voltage (V_{BIAS_P}) equal to 300 mV and a load resistance equal to 1 M Ω , is shown next in Fig 8.

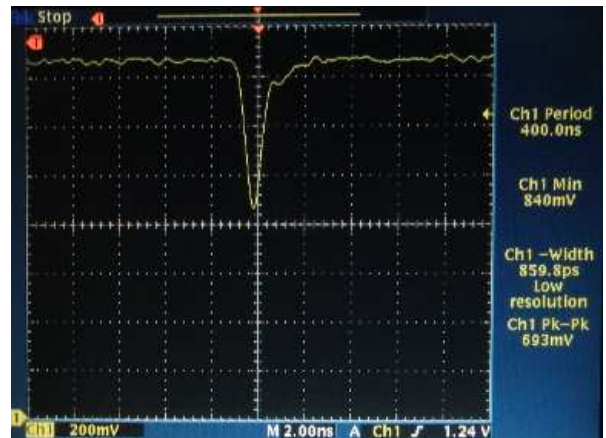


Figure 8. Output voltage of the short pulse generator circuit for Vref pulse=0.3 volt and a load resistance value of 1 Mohm.

The measured output voltage has a similar shape to the simulated output voltage of the short pulse generator circuit. It should be noted that the bandwidth of the oscilloscope is only 500 MHz, therefore the observed pulse shape is not exact. The pulse width and amplitude were measured using the oscilloscope, for different bias voltages values, the resulting values, as a function of the bias voltage and load resistance values are shown next in Fig. 9. and Fig. 10.

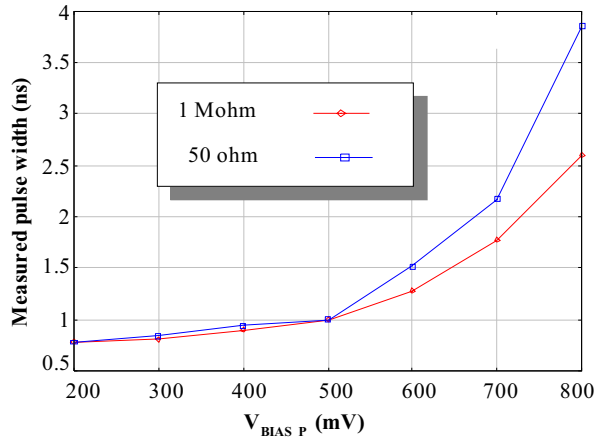


Figure 9. Measured pulse width as a function of the bias voltage for two different load values.

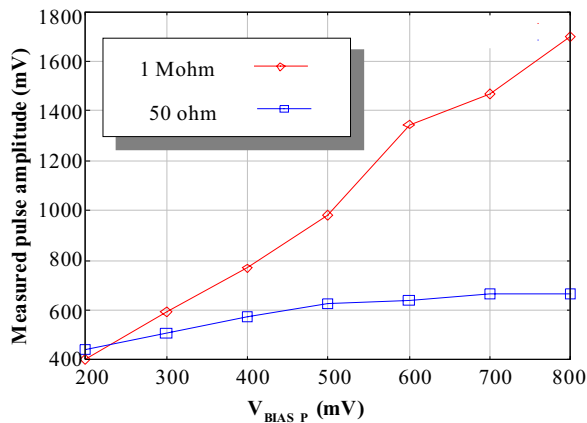


Figure 10. Measured pulse amplitude as a function of the bias voltage for two different load values.

The previous graphs show that the short-pulse generator circuit is capable of creating UWB short pulses with time duration between 0.7 ns and 3.5 ns. The pulse amplitude changes both with the control voltage and the load of the circuit. The amplitude of the pulse is smaller in the case of the 50 Ω load. These results are in agreement with the simulation results of the circuit.

Since the oscilloscope creates a vector with the sampled input voltages, the power spectral density (PSD) of the output pulse can be estimated applying the FFT to this vector, which was sampled with a sampling frequency of 5 GHz. The

resulting PSD of the output pulse when the V_{BIAS_P} is equal to 0.6 volt and the load resistance is 50 ohms, is shown next in Fig. 11. In this graph it is possible to observe the *sinc* modulation of the PSD of the output pulse.

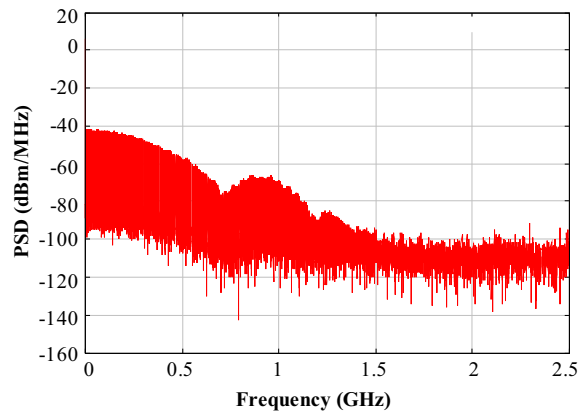


Figure 11. PSD of the output pulse for V_{Bias_P} =0.6 volt and a load resistance value equal to 50 ohms

V. CONCLUSIONS

This paper described a variable width short pulse generator circuit for UWB radar applications, built using 0.18 μm CMOS technology. This circuit is capable of generating pulses with a duration from 0.7 ns to 3.5 ns and an amplitude of 0.7 V with a 50 Ω load. The power supply voltage can be as low as 1.5 V and uses only 2.3 mA of power supply current.

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